Amendments to the Specification:

Please amend the paragraph beginning on page 10, line 24 as follows:

As depicted in FIG. 7, group circuit 144 includes a group G circuit 170, a group P circuit 171, and a group K circuit 172. Group G circuit 170 includes a series arrangement of three transmission gates 173, 174, and 175. Gate 173 receives an input signal g_b(0) representing the complement of the G signal in the 0th bit position and is gated by the p(1) signal resulting in an output that is TRUE only if g_b(0) and p(1) are TRUE. The output node of transmission gate 173 is also connected to Vcc through an NMOS transistor gated by the g(1) signal and further connected to ground through a PMOS transistor gated by k_b(1). The NMOS transistor will force the output node of transmission gate 173 to TRUE if g(1) is TRUE while the PMOS transistor will force the output to FALSE if k(1) is TRUE. Thus, the output node of transmission gate 173 is TRUE if g_b(0) AND p(1) OR g(1) {note that g(1) TRUE and k_b(1) FALSE are mutually exclusive states}. Second transmission gate 174 and third transmission gate 175 perform ~~an analogous function~~ **functions** for p(2) and p(3) ~~as~~ respectively ~~as~~ **that are analogous to the function that** first transmission gate 173 performs for p(1). The output node of each of the transmission gates is OR'd to Vcc through a NMOS transistor gated by the appropriate G bit according to the equations set forth in FIG. 4. In this manner, G circuit 171 calculates a group G value for bits 0 to 3 (or, by extension, for any other four bit grouping). The use of g_b(0) at the input inverts the result such that, after passing through inverting buffer 176, the appropriate polarity of G is achieved.

Amendments to the Abstract:

Please amend the Abstract as indicated:

An adder circuit for determining the sum of two operands including a set of PGK circuits, at least one tier of group circuits, and a carry generation circuit. The PGK circuits ~~are configured to~~ generate propagate, generate, and kill bits corresponding to at least a portion of the first and second operands. The group circuit receives propagate, generate, and kill bits from a plurality of the PGK circuits and produces a set of group propagate, generate, and kill values. The carry generation circuit receives a carry-in bit and the outputs of at least one of the group circuits and generates a carry-out bit representing the carry-out of the corresponding group. ~~Each generate bit is the logical AND of its corresponding bits in the first and second operand while each propagate bit is the EXOR of its corresponding bits, and each kill bit is the logical NOR of its corresponding bits. At least one of the~~ The PGK circuits, group circuits, and carry circuits may ~~be implemented with~~ use CMOS transmission gates in lieu of conventional complementary pass-gate logic (CPL). ~~The PGK circuits and groups may further generate true and complement output signals substantially simultaneously.~~